CLAIMS:

1. Modulation Code system comprising

an encoder (100) for transforming an original signal s into an encoded signal c satisfying predefined second constraints before the signal being transmitted via a channel (300) or stored on a recording medium; and

a decoder (200) for decoding the encoded signal c, after restoration, back into the original signal s;

wherein

the encoder (100) comprises a modulation code encoder (110) for transforming the original signal s into an intermediate signal t satisfying predefined first constraints and a transformer encoder (120) for transforming the intermediate signal t into the encoded signal c; and

the decoder (200) comprises a transformer decoder (220) for re-transforming the encoded signal c into said intermediate signal t and a modulation code decoder (210) for decoding said intermediate signal t into said original signal s.

2. An encoder (100) as part of the system as claimed in claim 1, comprising

the modulation code encoder (110) for transforming the original signal s into the intermediate signal t satisfying said predefined first constraints and

the transformer encoder (120) for transforming the intermediate signal t into the encoded signal c.

3. The encoder (100) according to claim 2, wherein the modulation code encoder (110) is an (0,k)-encoder.

4. The encoder (100) according to claim 2, wherein the encoder has a modulation code rate close to 1.

5. The encoder (100) according to claim 4, wherein the transformer encoder (120) has a modulation code rate close to or equal to 1.

6. The encoder (100) according to claim 2, wherein the transformer encoder (120) comprises

a shift-register (121) for defining a window for selecting a predetermined number of m+1 bits c_j-c_{j-m} from the serial encoded signal c and for outputting said selected m+1 bits c_j-c_{j-m} in parallel;

a computing logic (122) for logically combining the received parallel (m+1)-bits c_j-c_{j-m} output by said shift-register (121) into a logical output value; and

a logical XOR-Gate (123) for XOR combining the bits t_j of the received intermediate signal t with said logical output value in order to generate the bits c_j of said encoded signal c.

7. The encoder (100) according to claim 2, wherein the transformer encoder (120) is implemented in software or hardware.

8. Encoding method for transforming an original signal s into an encoded signal c satisfying predefined second constraints;

characterized by the following steps:

transforming the original signal s into an intermediate signal t satisfying predefined first constraints; and

transforming the intermediate signal t into the encoded signal c satisfying said second constraints.

9. A decoder (200) as part of the system as claimed in claim 1, characterized by the transformer decoder (220) for re-transforming the encoded signal c into said intermediate signal t; and the modulation code decoder (210) for decoding said intermediate signal t into said original signal c.

10. The decoder (200) according to claim 9, wherein the transformer decoder (220) is a sliding block decoder.

11. The decoder (200) according to claim 9, wherein the transformer decoder (220) comprises

a shift-register (221) for defining a window for selecting a predetermined

number of k+1 bits c_j-c_{j-k} from the received restored serial encoded signal c and for outputting said selected k+1 bits c_j-c_{j-k} in parallel; and

a decoding logic (222) for receiving and logically combining said parallel bits c_j-c_{j-k} from said restored encoded signal c in order to restore bits t_j of said intermediate signal t.

12. The decoder (200) according to claim 9, wherein the modulation code decoder (220) is a (0,k)-decoder.

13. The decoder (200) according to claim 9, wherein the decoder (200) has a modulation code rate close to 1.

14. The decoder (200) according to claim 13, wherein the transformer decoder (220) has a modulation code rate close to or equal to 1.

15. The decoder (200) according to claim 9, wherein the transformer decoder (220) is implemented in hardware or software.

16. Decoding method for decoding a restored encoded signal c satisfying predetermined second constraints into an original signal s

characterized by the following steps:

- re-transforming the restored encoded signal c into an intermediate signal t satisfying predetermined first constraints; and
- decoding the intermediate signal t into the original signal s.

17. The decoding method according to claim 16, wherein the step of re-transforming the encoded signal comprises the steps of:

a) determining the number k of consecutive bits c_j which must be considered in the restored encoded signal c in order to detect all specific patterns which are forbidden in the encoded signal according to said second constraints;

b) defining the window seize to k+1; and

c) determining a logic such that it transforms the k+1 bits c_j-c_{j-m} of the encoded signal c in the window - in the case that these k+1 bits c_j-c_{j-m} represent a forbidden pattern - into a bit value which corresponds to the value of the bit at the position k+2 of the encoded signal c.